## REMARKS

This paper is a preliminary amendment filed concurrently with a request for filing a continued prosecution application (CPA) for the above-captioned application. This preliminary amendment responds to the final Office Action mailed November 2, 1998 ("the Office Action"). Applicant respectfully requests reconsideration of the present application in light of the above amendments and the following remarks.

### *New Claims 17-20*

Claims 17-20 have been added. Applicant respectfully submits that the new claims are patentable over the prior art currently of record.

For a prior art reference to render a claim obvious, each claim element must be taught or suggested by the prior art, and each word in the claim must be considered in determining whether the claim is patentable over the prior art. MPEP 2143.03 (citing *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); and *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)). None of the prior art references teach or suggest each element of new independent claim 17. Claim 17 recites a buffer circuit that includes, among other things, a pass gate transistor having a drain receiving a first digital signal that varies between first and second voltage levels, a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on, a capacitor coupled across the source and drain of the pass gate transistor, an inverter receiving the output of the pass gate transistor, and a pull-up transistor having a source coupled to a second voltage supply, a drain coupled to the source of said pass gate transistor, and a gate coupled to the output terminal of said inverter.

None of the cited prior art references, alone or in combination, teach or suggest each of these elements. Regarding claim 17, the capacitor coupled across the source and drain of the pass gate transistor enhances the switching speed of a low-to-high transition while not negatively impacting the switching speed in a high-to-low transition equally. Regarding claim 18, the resistive element coupled between the first voltage supply and the gate of the pass gate transistor enhances the transition time of the output signal while providing electrostatic discharge protection. This enhanced transition time is accomplished through a "pumping" action of the parasitic capacitor located between the drain and gate of the pass gate transistor. The presence of the resistive element and the parasitic capacitor temporarily increase the voltage applied to the gate of the pass gate transistor during a low-to-high transition at the drain of the pass gate transistor.

Neither the Howell or Chown references discussed in the prior Office Actions include the structure claimed in independent claim 17 and the claims depending therefrom, nor do Howell or Chown teach or suggest a device that functions as the device claimed. Therefore, Applicant respectfully submits that new claims 17-20 are proper for allowance.

***35 U.S.C. § 103***

Section 3 of the Office Action rejected claims 1-16 under 35 USC 103(a) as being unpatentable over Howell or Chown. Applicant respectfully traverses these rejections.

Section 4 of the Office Action states that "since the claimed structure is fully met by the prior art of record (under 35 USC 103), the resulting function claimed by applicant will be inherent . . ." Applicant respectfully asserts that the claimed structure has not been met by either Howell or Chown.

As noted above, each claim element must be taught or suggested by the prior art. *In re Roika*. Claim 1, as amended, includes a resistive element having a first end portion coupled to the enable terminal of the transistor and a second end portion for coupling to a voltage supply to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to temporarily increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal. Neither Howell nor Chown teach or suggest using parasitic capacitance to enhance switching speed. The Howell and Chown references are not directed to buffer circuits; thus, there would be absolutely no motivation to modify either reference for the purpose of enhancing switching speed.

There must be some teaching, suggestion, or motivation to modify the teachings of the prior art in support of an obviousness rejection. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). The Office Action asserts that it would be obvious to add a resistive element between a voltage source and the transistor gate of Howell or Chown, for the purpose of setting the gate voltage at a level less than the bias voltage. First, there is no suggestion in either Howell or Chown of adding a resistor between a voltage supply and the gate for any purpose, and more specifically, for the purpose of establishing a lower bias voltage. Further, there is absolutely no suggestion of adding a resistive element that cooperates with a parasitic capacitor to enhance switching speed.

Moreover, claim 1 states that the transistor is biased continuously on. There is certainly no suggestion of biasing the devices disclosed in Howell or Chown continuously on, and it appears that the devices disclosed in Howell and Chown would not function properly if biased in

this manner. If a modification of a prior art device would render it unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Thus, Applicant contends that there is no motivation in either Howell or Chown to bias the transistors disclosed therein as recited in claim 1 of the present application.

Similarly, independent claims 1, 8, 13, and 15, as amended, each recite receiving and delivering signals that vary between preselected levels -- i.e., logically high and low signals. For example, claims 1 and 13 recite receiving signals that vary between first and second preselected voltage levels and delivering signals that vary between the first preselected voltage level and a third preselected voltage level. Claims 8 and 15 refer to converting digital signals that vary between 0 volts and a first preselected voltage level to digital signals that vary between 0 volts and a second preselected voltage level.

The devices disclosed in Howell and Chown do not receive or deliver digital signals, and there is no motivation in either reference for modifying the devices disclosed therein for transmitting digital data. Howell is directed to an arcless circuit interrupter for reducing the arc that occurs between separating contacts within a protected circuit. The purpose of the circuit disclosed in Howell is to "describe a circuit which completely eliminates the occurrence of an arc between separating contacts both under ordinary circuit conditions as well as upon the occurrence of an overload condition." Howell at col. 1, lines 54-58. Howell provides an "impedance circuit," which in the embodiment illustrated in Figure 3, includes an FET. A control circuit biases the impedance circuit normally on, allowing current to flow through the impedance circuit. When it is desired to interrupt the circuit current, bias is removed from the

impedance circuit to increase the impedance thereof to divert the current through the current interrupter.

Any modification to the circuit shown in Figure 3 of Howell such that digital signals are applied to the drain of the FET (23) and delivered by the source would fundamentally change the function of the disclosed circuit, making it unsatisfactory for its intended purpose. Similarly, Chown discloses an optical receiver that includes a FET, which, among other things, has its source terminal connected to ground. Thus, the output terminal, or source, is not for delivering digital signals. Modifying the circuit disclosed in Chown such that its drain receives digital signals and its source delivers digital signals, would result in the device being unsatisfactory for its intended purpose.

Applicant respectfully submits that there is no motivation for modifying the disclosures of Howell or Chown such that they convert digital signals from one value to another. Therefore, Applicant believes that independent claims 1, 8, 13, and 15, as well as the claims depending therefrom, are proper for allowance.

Moreover, dependent claims 2 - 5 include the element of a buffer circuit coupled to receive signals from the transistor output terminal. Neither Howell nor Chown disclose or suggest a buffer circuit coupled to the output of the transistors disclosed therein. Thus, Applicant respectfully submits that neither Howell nor Chown can render claims 2 - 5 unpatentable. Still further, as discussed above, Howell discloses an arcless circuit interrupter and Chown discloses an optical receiver. As the FETs disclosed in Howell and Chown are not provided for transmitting digital signals, there would be no reason to couple a buffer circuit to the output of the FETs disclosed in Howell and Chown.

For these reasons, Applicant respectfully submits that claims 1-16, as amended, are patentable over Howell and Chown.

## CONCLUSION

Applicant has offered the above amendments and remarks in a genuine effort to advance this case towards issuance. Therefore, reconsideration of these claims is respectfully requested.

If the Examiner believes that a telephone conference would be beneficial to advance this case towards allowance, he is strongly encouraged to telephone the undersigned at the number provided below.

Should any fees (in addition to those submitted with the CPA request filed herewith) under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Assistant Commissioner is authorized to deduct said fees from Arnold White & Durkee Deposit Account No. 01-2508/INPA:035/GLE.

Respectfully submitted,

Date: 2/2/99

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